INFORMATION DISCLOSURE STATEMENT

Atty. Docket No. 1490	Serial No. 10/015865
Applicant: SARTSCHEV, Ronald A., et al.	
Filing Date: 12/12/2001	Group: 2133

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if appropriate
TSP	AA	6285963	Sep 4, 2001	West	702	117	Nov 30, 1999
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		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
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TSP	AJ	MOTA, M. et al.: "A flexible multi-channel high-resolution time-to-digital converter ASIC", 2000 IEEE Nuclear Science Symposium. Conference Record (Cat. No. OOCH37149), 2000 IEEE Nuclear Science Symposium. Conference Record, Lyon, France, 15-20 Oct. 2000, vol.2, pages 9/155-9 189, XP002236607 2000, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-6503-8, page 9-155, page 9-158
TSP	AK	MOTA, M. et al: "A four-channel self-calibrating high-resolution time to digital converter" Electronics, Circuits and Systems, 1998, IEEE International Conference on Lisboa, Portugal 7-10 Sept. 1998, Piscataway, NJ, USA, IEEE, US, 7 Sept 1998 (1998-09-07), pages 409-412, XP010366204, ISBN: 0-7803-5008-1, page 409, page 410
TSP	AL	CHRISTIANSEN J.: "An integrated high resolution CMOS timing generator based on an array of delay locked loops", IEEE Jounal of Solid0State Circuits, IEEE Inc. New York, US, vol. 31, no. 7, 1 July 1996 (1996-07-01), pages 952-957, XP000632381, ISSN: 0018-9200, the whole document
	AM	
	AN	
	AO	

Examiner	THANH S. PHAN	Date Considered	9/07/04

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INFORMATION DISCLOSURE STATEMENT

Atty. Docket No. 1499	Serial No. 10/015865
Applicant: SARTSCHEV, Ronald A., et al.	
Filing Date: 12/12/01	Group:

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if appropriate
TSP	AA	6,246,737	Jun 12, 2001	Kuglin	375	371	Oct 26, 1999
TSP	AB	5,694,377	Dec 2, 1997	Kushnick	368	120	Apr 16, 1996
TSP	AC	6,073,259	Jun 6, 2000	Sartschev et al.	714	724	Aug 5, 1997
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TSP	AJ	Rainer Geiges, et al., "A High Resolution TDC Subsystem," IEEE Transactions on Nuclear Science, Vol. 41, No. 1, February 1, 1994
	AK	M. Sugawara, et al. "A 2.5V 100MS/s 8bit ADC Using Pre-Linearization Input Buffer and Level Up DAC/Subtractor," 1998 Symposium on VLSI Circuits Digest of Technical Papers, August 1998
	AL	J. Christiansen, "An Integrated CMOS 0.15 ns Digital Timing Generator for TDS's and Clock Distribution Systems," March 1995
	AM	Piotr Dudek, et al., "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," IEEE Transactions on Solid-State Circuits, Vol. 35, No. 2, February 2000
	AN	Yasuo Arai, et al., "A CMOS Four-Channel X 1K Time Memory LSI with 1-ns/b Resolution," IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March 1992
TSP	AO	Andrew E. Stevens, et al., "A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989

Examiner	THANH S. PHAN	Date Considered	2/07/04

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TSP	AJ	C. Thomas Gray, et al., "A Sampling Technique and Its CMOS Implementation with 1 Gb/s Bandwidth and 25 ps Resolution," IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, March 1994
	AK	Keunoh Park, et al., "20ps Resolution Time-to-Digital Converter for Digital Storage Oscilloscopes," September 1999
	AL	Joonbae Park, et al., "An Auto-Ranging 50-210Mb/s Clock Recovery Circuit with a Time-to-Digital Converter," 1999 IEEE International Solid-State Circuits Conference, February 17, 1999
	AM	Elvi Raisanen-Ruotsalainen, et al., "An Integrated Time-to-Digital Converter with 30-ps Single-Shot Precision," IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000
	AN	R. Rankinen, et al., "Time-to-Digital Conversion with 10 ps Single Shot Resolution," 1991
TSP	AO	Elvi Raisanen-Ruotsalainen, et al., "A BiCMOS Time-to-Digital Converter with 30 ps Resolution," 1999

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TSP	AJ	Elvi Raisanen-Ruotsalainen, et al., "A Low-Power CMOS Time-to-Digital Converter," IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
	AK	Hideki Shirasu, et al., "A VME 32 Channel Pipeline TDC Module with TMC LSIs," IEEE Transactions on Nuclear Science, Vol. 43, No. 3, June 1996
	AL	J. Kalisz, et al., "Time-to-Digital Converter with Direct Coding and 100ps Resolution," Electronics Letters, Vol. 31, No. 19, September 14, 1995
	AM	Dinis M. Santos, et al., "A CMOS Delay Locked Loop and Sub-Nanosecond Time-to-Digital Converter Chip," 1996
	AN	Antti Mantyniemi, et al., "A High Resolution Digital CMOS Time-to-Digital Converter Based On Nested Delay Locked Loops," 1999
TSP	AO	Timo E. Rahkonen, et al., "The Use of Stabilized CMOS Delay Lines for the Digitization of Short Time Intervals," IEEE Journal of Solid-State Circuits, Vol. 28, No. 8, August 1993

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TSP	AJ	Timo Rahknone, et al., "Time Interval Measurements Using Integrated Tapped CMOS Delay Lines," 1990
	AK	P. Bailly, et al., "A 16-Channel Digital TDC Chip,"
	AL	Vadim Gutnik, et al., "On-Chip Picosecond Time Measurement," 2000 Symposium on VSLI Circuits Digest of Technical Papers, April 2000
	AM	Jozef Kalisz, et al., "Single-Chip Interpolating Time Counter With 200-ps Resolution and 43-s Range," IEEE Transactions on Instrumentation and Measurement, Vol. 46, No. 4, August 1997
	AN	C. Ljuslin, et al., "An Integrated 16-Channel CMOS Time to Digital Converter," IEEE Transactions on Nuclear Science, Vol. 41, No. 4, August 1994
TSP	AO	Beomsup Kim, et al., "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-um CMOS," IEEE Journal of Solid-State Circuits, Vol. 25, No. 6, December 1990

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TSP	AJ	"Misfire Analysis with Time Interval Analyzer," Yokogawa Test and Measurement, wysiwyg://210/http://www.yokogawa.com/tm/appli/48/48misfire.html
TSP	AK	"Using FastFrame Segmented Memory," Tektronix MBD: Applications, sysiyg://BODY.181/http://www.tektronix...easurement/App_Notes/dpo/fastframe/eng/
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Examiner	THANH S. PHAN	Date Considered	02/07/04

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